PEREGRINE SEMICONDUCTOR

PRODUCT SPECIFICATION

PE4237

SPDT High Power MOSFET RF Switch

Features

- Single 3.0-volt power supply
- Low insertion loss: 0.35 dB at 1.0 GHz, 0.45 dB at 2.0 GHz
- High isolation of >43 dB at 1.0 GHz, >35 dB at 2.0 GHz
- Typical 1 dB compression point of +32 dBm
- Single-pin CMOS or TTL logic control
- Small 3x3mm MLPM package

Product Description

The PE4237 High Power MOSFET RF Switch is designed to cover a broad range of applications from DC through 4.0 GHz. This reflective switch integrates on-board CMOS control logic driven by a single-pin, low voltage CMOS or TTL control input. Using a nominal +3-volt power supply, a 1 dB compression point of +32 dBm can be achieved. The PE4237 also exhibits outstanding isolation of better than 43 dB at 1.0 GHz and is offered in a small 3x3mm MLPM package.

The PE4237 High Power MOSFET RF Switch is manufactured in Peregrine's patented Ultra Thin Silicon (UTSi®) CMOS process, offering the performance of GaAs with the economy and integration of conventional CMOS.

Figure 1. Functional Schematic Diagram

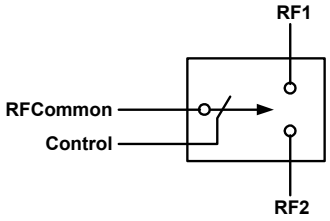


Figure 2. Package Type

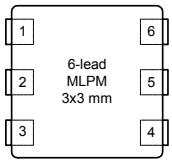


Table 1. Electrical Specifications @ +25 °C, V_{DD} = 3 V (As measured in a 50 Ω system)

Parameter	Conditions	Minimum	Typical	Maximum	Units
Operation Frequency[1]		DC		4000	MHz
Insertion Loss	1000 MHz 2000 MHz		0.35 0.45	0.50 0.60	dB dB
Isolation – RFCommon to RF1/RF2	1000 MHz 2000 MHz	41 33	43 35		dB dB
Isolation – RF1 to RF2	1000 MHz 2000 MHz	33.5 26.5	35 28		dB dB
Return Loss	1000 MHz 2000 MHz	19 10.5	24 14		dB dB
'ON' Switching Time	50% CTRL to 0.1 dB final value, 2 GHz		200		ns
'OFF' Switching Time	50% CTRL to 25 dB isolation, 2 GHz		90		ns
Video Feedthrough[2]			15		mV_{pp}
Input 1 dB Compression	2000 MHz	30	32		dBm
Input IP3	2000 MHz, 17 dBm	50			dBm

Notes: 1. Device linearity will begin to degrade below 10 MHz.

2. The DC transient at the output of any port of the switch when the control voltage is switched from Low to High or High to Low in a 50Ω test set-up, measured with 1ns risetime pulses and 500 MHz bandwidth.

Figure 3. Pin Configuration (Top View)

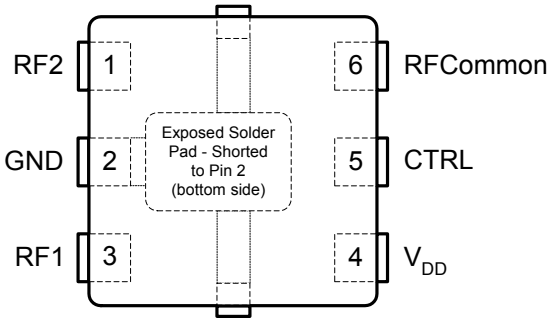


Table 2. Pin Descriptions

Pin No.	Pin Name	Description
1	RF2	RF2 port.[1]
2	GND	Ground Connection. Traces should be physically short and connected to the ground plane. This pin is connected to the exposed solder pad that also must be soldered to the ground plane for best performance.
3	RF1	RF1 port.[1]
4	V_{DD}	Nominal 3 V supply connection.
5	CTRL	CMOS or TTL logic level: High = RFCommon to RF1 signal path Low = RFCommon to RF2 signal path
6	RF Common	Common RF port for switch.[1]

Note 1: All RF pins must be DC blocked with an external series capacitor or held at $0V_{DC}$.

Table 3. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Units
V_{DD}	Power supply voltage	-0.3	4.0	V
V_I	Voltage on any input except for the CTRL input	-0.3	V_{DD}+ 0.3	V
V_{CTRL}	Voltage on CTRL input		5.0	V
T_{ST}	Storage temperature range	-65	150	°C
T_{OP}	Operating temperature range	-40	85	°C
P_{IN}	Input power (50Ω)		35	dBm
V_{ESD}	ESD voltage (Human Body Model)		250	V

Table 4. DC Electrical Specifications

Parameter	Min	Typ	Max	Units
V_{DD} Power Supply Voltage	2.7	3.0	3.3	V
I_{DD} Power Supply Current (V_{DD} = 3V, V_{CNTL} = 3V)		29	35	μA
Control Voltage High	0.7xV_{DD}			V
Control Voltage Low			0.3xV_{DD}	V

Control Logic Input

The control logic input pin (CTRL) is typically driven by a 3-volt CMOS logic level signal. For flexibility to support systems that have 5-volt control logic drivers, the control logic input has been designed to handle a standard 5-volt TTL control signal. This TTL control signal input must not exceed 5-volts or damage to the switch could result.

Table 5. Control Logic Truth Table

Control Voltage	Signal Path
CTRL = CMOS or TTL High	RFCommon to RF1
CTRL = CMOS or TTL Low	RFCommon to RF2

Electrostatic Discharge (ESD) Precautions

When handling this UTSi device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified.

Latch-Up Avoidance

Unlike conventional CMOS devices, UTSi CMOS devices are immune to latch-up.

Typical Performance Data @ -40 °C to 85 °C (Unless Otherwise Noted)

Figure 4. Insertion Loss – RFC to RF1

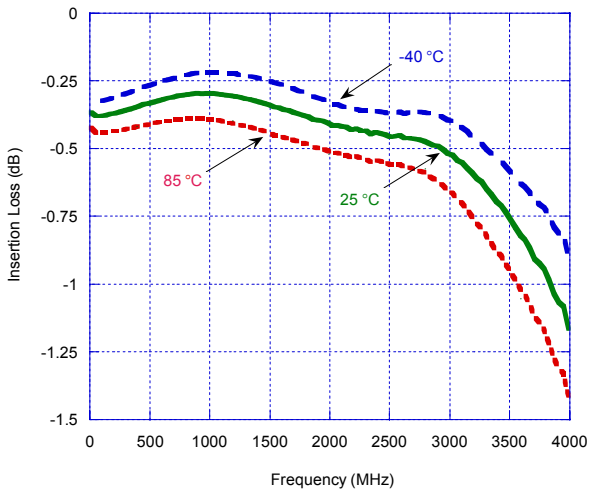


Figure 5. Input 1dB Compression Point

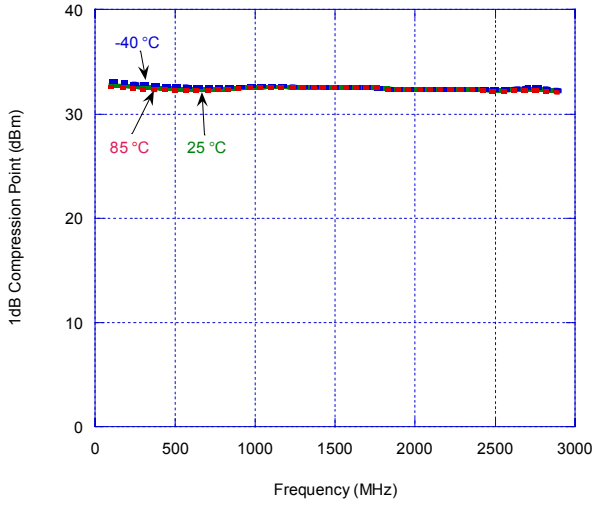


Figure 6. Insertion Loss – RFC to RF2

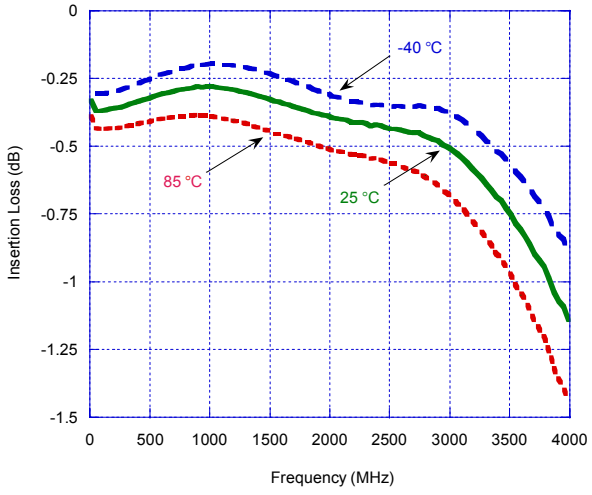
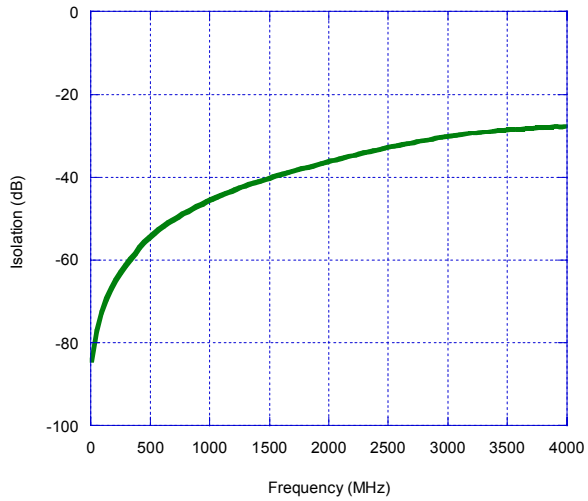


Figure 7. Isolation – RFC to RF1



Typical Performance Data @ -40 °C to 85 °C (Unless Otherwise Noted)

Figure 8. Isolation – RFC to RF2

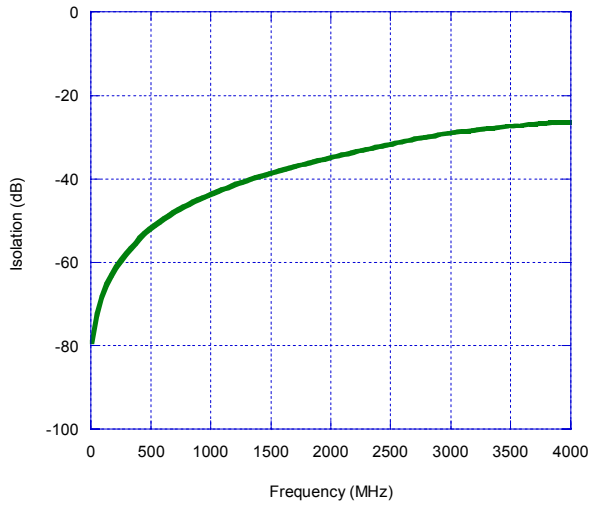


Figure 9. Isolation – RF1 to RF2, RF2 to RF1

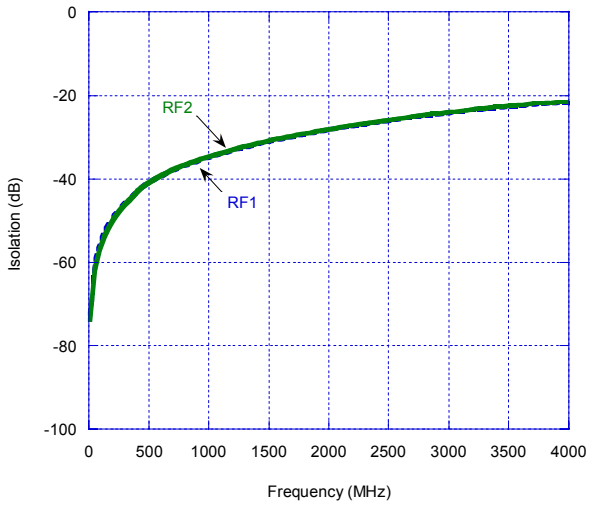


Figure 10. Return Loss – RFC

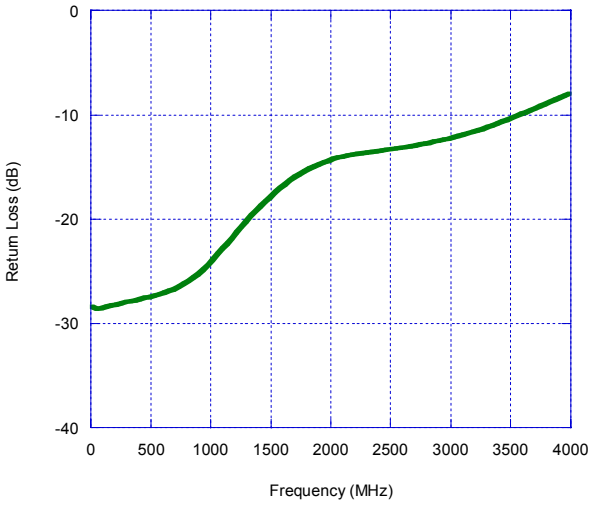
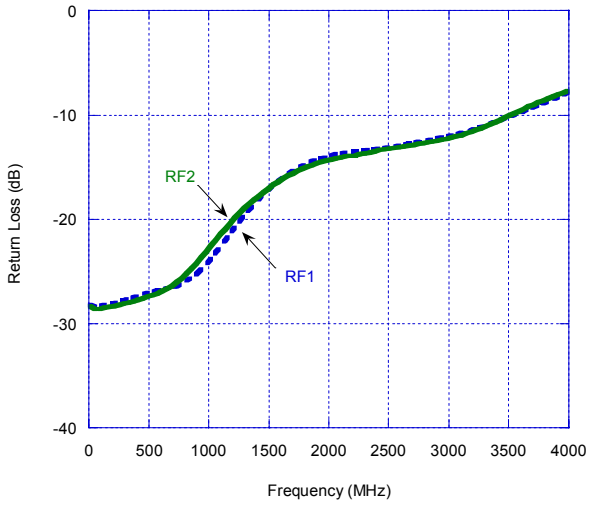


Figure 11. Return Loss – RF1, RF2



Evaluation Kit Information

Evaluation Kit

The SPDT Switch Evaluation Kit board was designed to ease customer evaluation of the PE4237 SPDT switch. The RF common port is connected through a 50Ω transmission line to the top left SMA connector, J1. Port 1 and Port 2 are connected through 50Ω transmission lines to the top two SMA connectors on the right side of the board, J2 and J3. A through transmission line connects SMA connectors J4 and J5. This transmission line can be used to estimate the loss of the PCB over the environmental conditions being evaluated.

The board is constructed of a two metal layer FR4 material with a total thickness of 0.031". The bottom layer provides ground for the RF transmission lines. The transmission lines were designed using a coplanar waveguide with ground plane model using a trace width of 0.0476", trace gaps of 0.030", dielectric thickness of 0.028", metal thickness of 0.0021" and ε_r of 4.4.

J6 provides a means for controlling DC and digital inputs to the device. Starting from the lower left pin, the second pin to the right (J6-3) is connected to the device CNTL input. The fourth pin to the right (J6-7) is connected to the device V_{DD} input. A decoupling capacitor (100 pF) is provided on both CNTL and V_{DD} traces. It is the responsibility of the customer to determine proper supply decoupling for their design application. Removing these components from the evaluation board has not been shown to degrade RF performance.

Figure 12. Evaluation Board Layouts

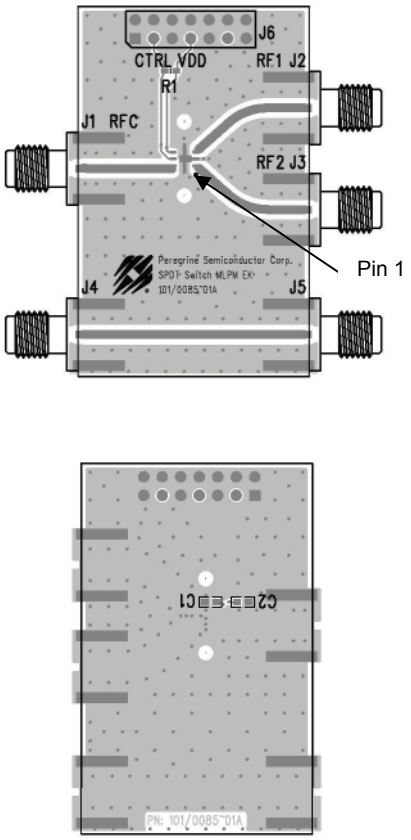


Figure 13. Evaluation Board Schematic

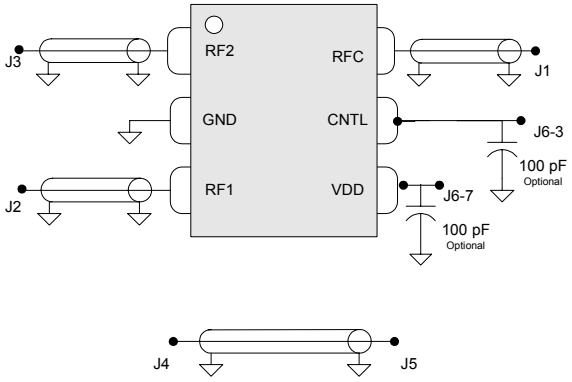
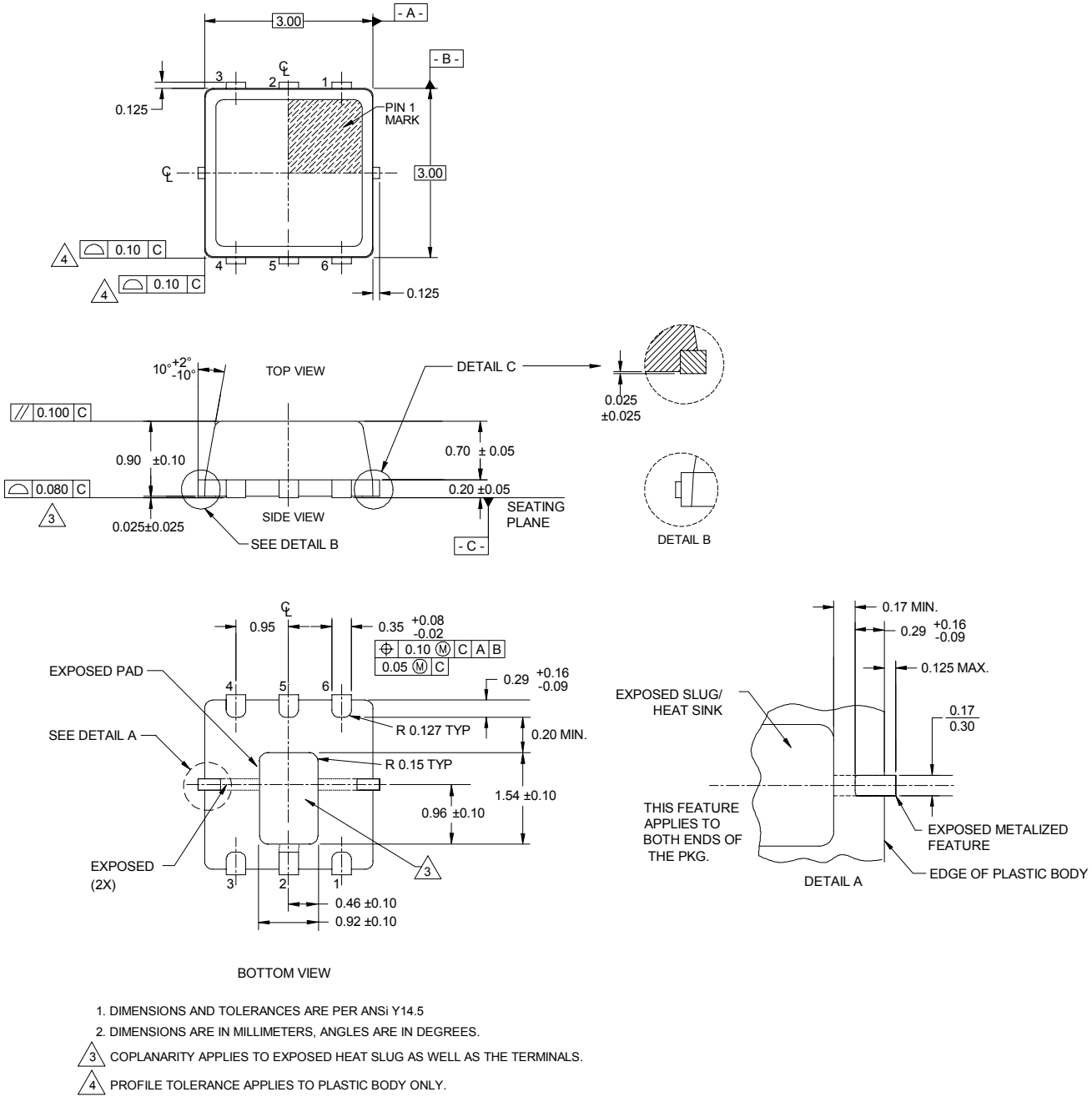


Figure 14. Package Drawing

6-lead MLPM



1. DIMENSIONS AND TOLERANCES ARE PER ANSi Y14.5
2. DIMENSIONS ARE IN MILLIMETERS, ANGLES ARE IN DEGREES.
3. COPLANARITY APPLIES TO EXPOSED HEAT SLUG AS WELL AS THE TERMINALS.
4. PROFILE TOLERANCE APPLIES TO PLASTIC BODY ONLY.

Table 6. Ordering Information

Order Code	Part Marking	Description	Package	Shipping Method
4237-01	4237	PE4237-06MLP3x3-12800F	6-lead 3x3mm MLPM	12800 units / Canister
4237-02	4237	PE4237-06MLP3x3-3000C	6-lead 3x3mm MLPM	3000 units / T&R
4237-00	PE4237-EK	PE4237-06MLP3x3-EK	Evaluation Board	1 / Box

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For a list of representatives in your area, please refer to our Web site at: ***http://www.peregrine-semi.com***

Data Sheet Identification

Advance Information

The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The data sheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The data sheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a PCN (Product Change Notice).

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Peregrine products are protected under one or more of the following U.S. patents: 6,090,648; 6,057,555; 5,973,382; 5,973,363; 5,930,638; 5,920,233; 5,895,957; 5,883,396; 5,864,162; 5,863,823; 5,861,336; 5,663,570; 5,610,790; 5,600,169; 5,596,205; 5,572,040; 5,492,857; 5,416,043. Other patents are pending.